Application No.: 09/638,268 Atty. Docket No.: 20421-00074-US

REMARKS

Claims 1-21 are pending in the application.

Withdrawal of the rejection of claims 20 and 21 under 35 U.S.C. § 112 is requested. The rejected claims are supported on page 10 of the specification. Lines 17-22 include the recitation:

> In order to systematically enumerate each possible parameter combination, the generator assigns a significance level to each parameter combination specification in a *command* statement, based on its place in a sequence within the *command* statement. In an embodiment, the parameter combination specification last in the sequence is the least significant, the next-to-last parameter combination specification is next-to-least significant, and so on up to the first or most significant specification in the sequence.

It is clear that this portion of the specification fully supports claims 20 and 21. In fact, the language of claims 20 and 21 has been essentially lifted from this portion of the specification.

Withdrawal of the rejection of claims 1, 3-5 and 7 under 35 U.S.C. § 103 as being unpatentable over Hellestrand et al. (U.S. Pat. No. 6,263,302) in view of Apostol, Jr. et al. (U.S. Pat. No. 6,247,084) and Sheafor et al. (U.S. Pat. No. 6,321,285) and further in view of Huggins (U.S. Pat. No. 5,956,478) is requested. The present invention is directed to a method and system for generating test cases representing bus transactions of a device under test. The bus transactions can then be applied to a simulator to emulate a bus protocol for a design under test modeled by hardware description language.

As noted in the previous response, a configuration file is prepared which describes a device under test in terms of bus transactions that it performs. The condensed configuration file is then used to generate all the bus transactions based on various parameter combinations stored in the configuration file. The bus transactions comprise an output file which is used in the bus simulator to determine if the device under test completely complies with the standardized bus interface.

Turning to claim 1 specifically, the invention requires that there be a design under test configuration file comprising the specification of bus transaction types and parameters corresponding to the design under test. The configuration file is processed to generate a test case comprising bus transactions which verify the design under test.

As acknowledged in the Office Action, Hellestrand et al. (U.S. Pat. No. 6,263,302), the primary reference cited in the rejection fails to disclose any design under test configuration file as set forth in rejected claim 1, comprising a specification of transaction types and parameters corresponding to the device under test. The Office Action, however, alleges that the Apostol, Jr. et al. (U.S. Pat. No. 6,247,084) reference discloses such a configuration file.

Turning now to the Apostol, Jr. et al. (U.S. Pat. No. 6,247,084) reference, a unified memory system is disclosed which has first and second multi-bit bi-directional system buses. By incorporating two separate busses, latency is reduced from accessing an external memory through the memory controller. The dual internal bus architecture reduces performance bottlenecks. The reference does not disclose any system for generating test cases for a design under test. There are no configuration files disclosed which would constitute a specification of any bus transaction type, and any parameters corresponding to a design under test. The references are totally unrelated to any testing of any design and are, instead, directed to providing improved access to an external memory by using a multiple bus architecture between a memory controller and a plurality of bus transaction circuits, and between the processor and memory controller.

The Sheafor et al. (U.S. Pat. No. 6,321,285) reference describes a bus arrangement for interconnecting a number of discrete and/or integrated modules in a digital system. The system provides a particular type of addressing and data transaction scheme, where a series of address transactions may be performed between modules which are interconnected by a bus, so that each address transaction defines an associated data transaction. The data transaction can thereafter be performed on the same bus arrangement in a sequence which is different from the order in which the address transaction was performed. This reference, as well, does not in any way disclose a design under test configuration file as claimed in the present application.

Turning now to the Huggins (U.S. Pat. No. 5,956,478) reference, a system for generating test cases for testing a processor is disclosed. The system is designed to avoid the condition of an infinite testing loop because of branching instructions being executed. Thus, test cases are generated which comprise blocks of instructions that can have only one branch path to it. Therefore, the execution can be transferred to a different block without the risk of entering a branching path which would result in an infinite testing loop.

The concept of a configuration file, for generating a test case, comprising bus transactions to verify a design under test is totally absent from the cited reference which is directed to a system for creating test instructions which avoids the formation of an infinite loop.

Withdrawal of the rejection of claims 2, 6, 8, 10 and 11 under 35 U.S.C. § 103 as being unpatentable over Hellestrand et al. (U.S. Pat. No. 6,263,302) in view of Apostol, Jr. et al. (U.S. Pat. No. 6,247,084) and Sheafor et al. (U.S. Pat. No. 6,321,285) further in view of Huggins (U.S. Pat. No. 5,956,478) and Shrote (U.S. Pat. No. 5,774,358) is requested. Each of the rejected claims is directed to a method for generating test cases for verifying a design under test. The method includes describing the device under test in a configuration file and converting the contents of the configuration file to a test case comprising bus transactions. In particular, claims 2 and 6 require that rules of the configuration file be evaluated to include or exclude selected ones of the bus transactions from the test case.

The addition of the Shrote (U.S. Pat. No. 5,774,358) reference to the previously noted references fails to disclose this subject matter. In reviewing the Shrote reference, there is no reference to a configuration file which is used to create test cases comprising bus transactions. The concept of having rules to include or exclude selected ones of the bus transactions from the test case is not suggested in any of the foregoing references.

Withdrawal of the rejection of claim 9 under 35 U.S.C. § 103 as being unpatentable over Hellestrand et al. (U.S. Pat. No. 6,263,302) in view of Apostol, Jr. et al. (U.S. Pat. No. 6,247,084), Sheafor et al. (U.S. Pat. No. 6,321,285) and further in view of Huggins (U.S. Pat. No. 5,956,478), Shrote (U.S. Pat. No. 5,774,358) and Mantooth et al. (U.S. Pat. No. 6,236,956) is respectfully requested. Claim 9 is dependent on claim 8. Each of these claims all depend from claim 5 which calls for a configuration file which describes using a condensed syntax a design under test. Claim 8 specifically calls for a syntax which specifies transaction types, a set of parameters for each transaction type and directives for converting the condensed syntax into a number of possible parameter combinations. Each of the foregoing references fails to disclose any such configuration file or test case which is derived by converting the condensed syntax of the configuration file to a test case.

Withdrawal of the rejection of claims 12-14 under 35 U.S.C. § 103, as being unpatentable over Hellestrand et al. (U.S. Pat. No. 6,263,302) in view of Apostol, Jr. et al. (U.S. Pat. No. 6,247,084) and Sheafor et al. (U.S. Pat. No. 6,321,285) further in view of Shrote (U.S. Pat. No. 5,774,358) and further in view of Meyer (U.S. Pat. No. 6,571,204) is requested. Claims 12-14 are computer product claims which execute the processes of claims 1 and 5. These claims include steps for evaluating a syntax of a configuration file including statements defining transaction types and parameters corresponding to the device under test, as well as generating bus functional language statements from the syntax. None of the foregoing references provide any disclosure for generating bus functional language statements from the syntax. Accordingly, it is not seen how there can be any combination of the references which will suggest this aspect of the claims.

Withdrawal of the rejection of claims 15, 16, 18 and 19 under 35 U.S.C. § 103 as being unpatentable over Hellestrand et al. (U.S. Pat. No. 6,263,302) in view of Apostol, Jr. et al. (U.S. Pat. No. 6,247,084) and Sheafor et al. (U.S. Pat. No. 6,321,285) and further in view of Shrote (U.S. Pat. No. 5,774,358) is requested. The rejected claims are system claims, including limitations which are related to the method claims previously discussed. Each of the system claims requires a configuration file for a device under test including bus transaction types and parameters corresponding to the device under test. The instructions process the configuration file to generate bus transactions to verify the device under test. None of the foregoing references provide for any such configuration files for use in such a system.

Withdrawal of the rejection of claim 17 under 35 U.S.C. § 103 as being unpatentable over Hellestrand et al. (U.S. Pat. No. 6,263,302) in view of Shrote (U.S. Pat. No. 5,774,358) is requested. Claim 17 is directed to a method for generating a test case to a bus interface. The configuration file of the foregoing claims is formed of parameter combinations in condensed syntax. The configuration file includes commands and rules to select various parameter combinations to be included and/or excluded from a test case. The configuration file is then used to generate bus transactions which are used in a bus simulator.

As was noted previously, Hellestrand et al. (U.S. Pat. No. 6,263,302) discloses a type of simulator wherein some of the operations of a target processor bus may be simulated by running a bus hardware model on the hardware simulator. The disclosed system simulates the effects of a design on the bus hardware. However, the reference fails to disclose any method or apparatus to generate test cases to completely test a design under test. The formation of a configuration file as set forth in the rejected claims, of various parameter combinations, in creating bus transactions from the configuration files, does not appear to be shown in Hellestrand et al. (U.S. Pat. No. 6,263,302). Thus, that feature of the Applicants claims directed to creating a configuration file is not disclosed in any of the cited references (page 6 of the Office Action recognizes the fact that Hellestrand et al. does not teach any configuration file which comprises a specification of bus transaction types and parameters corresponding to the device under test).

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In view of the foregoing, wherein it has been demonstrated that various limitations throughout Applicants' claims are not disclosed in the references, favorable reconsideration is believed to be in order.

Applicant believes no fee is due with this response. However, if a fee is due, please charge our Deposit Account No. 09-0464, under Order No. RAL9-2000-0069-US1 from which the undersigned is authorized to draw.

Dated: 7/29/04

Respectfully submitted,

By _____

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